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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application / Conf. No.	10/618,316 / 4779
		Filing Date	July 11, 2003
		First Named Inventor	Patrick Lysaght
		Art Unit	2825
		Examiner Name	Vuthe Siek
		Attorney Docket Number	X-1410 US
Sheet	2	of	2

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
VS		Monica Alderighi et al.; "A Fault-Tolerant FPGA-Based Multi-Stage Interconnection Network for Space Applications"; published Computer Society; pp. 1-5. (No date)	
VS		Ian Kyles; "Creating Large Switch Fabrics using the Three-Stage (Clos) Architecture"; Copyright VITESSE Semiconductor Corporation; pp. 1-12. (No date)	
VS		Steve Young et al.; "A High I/O Reconfigurable Crossbar Switch"; pp. 1-8. (No date)	

Examiner Signature	VUTHE SIEK	Date Considered	7/11/03
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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